What is claimed is:

1. A method of inserting a test point into a circuit design, comprising :

selecting a node in said circuit design;

determining a driver cell of said node;

selecting from a file, a replacement cell for said driver cell, said replacement cell having the same function of said driver cell and a test point function; and

replacing said driver cell in said circuit design with said replacement cell.

2. The method of claim 1 wherein said circuit design has signal propagation delay limits and the signal propagation delay of said circuit design with said replacement cell is within said signal propagation delay limits of said circuit design.

3. The method of claim 1, wherein said test point function of said replacement cell is a control to zero, control to one or observe function.

4. The method of claim 1, wherein said file is a replacement table.

5. The method of claim 1, wherein said file is the design library used to create said circuit design.

6. A method of inserting a test point into a circuit design, comprising :

selecting said test point to be inserted into said circuit design, said circuit design having signal propagation delay limits;

determining a driver cell of the test point;

selecting from a file, a replacement cell for said driver cell, said replacement cell having the same function of said driver cell and a test point function;

determining the delay of said circuit design with said replacement cell; and

replacing said driver cell with said replacement cell if the delay of said circuit design with said replacement cell is within said signal propagation delay limits.

7. The method of claim 6, further including :

determining the delay of said circuit design with said driver cell; and

applying a predetermined range to the delay of said circuit design with said driver to create said signal propagation limits.

8. The method of claim 6, wherein said test point function of said replacement cell is a control to zero, control to one or observe function.

9. The method of claim 6, wherein said file is a replacement table.

10. The method of claim 6, wherein said file is the design library used to create said circuit design.

11. The method of claim 9, wherein said replacement table comprises:

a list of driver cells comprised of at least a portion of the gates in the design library used to create said circuit design;

a combination of each of said gates in said list of driver cells and a control to zero function;

a combination of each of said gates in said list of driver cells and a control to one function; and

a combination of each of said gates in said list of driver cells and an observe function.

12. The method of claim 11, wherein said replacement table further comprises gates in addition to gates in said design library including:

one or more combinations of gates not in said design library and a control to zero function;

one or more combinations of a gates not in said design library and a control to one function; and

one or more combinations of a gates not in said design library and an observe function.

13. A method of inserting a test point into a circuit design, comprising :

selecting a test point to be inserted into said circuit design, said circuit design having signal propagation delay limits;

determining a driver cell of the test point;

selecting from a file, all potential replacement cells for said driver cell, said potential replacement cells having the same function of said driver cell and a test point function;

determining the delay of said circuit design with each of said potential replacement cells;

adding to an accept list those replacement cells where the delay of said circuit design with said potential replacement cell is within said signal propagation delay limits;

selecting a replacement cell from said accept list; and

replacing said driver cell with said replacement cell.

14. The method of claim 13, further including :

determining the delay of said circuit design with said driver cell; and

applying a predetermined range to the delay of said circuit design with said driver to create said signal propagation limits.

15. The method of claim 13, further including the step of:

performing an early and a late mode analysis of said circuit design with said driver to determine said signal propagation delay limits.

16. The method of claim 13, wherein said test point function of said replacement cell is a control to zero, control to one or observe function.

17. The method of claim 13, wherein said file is a replacement table.

18. The method of claim 13, wherein said file is the design library used to create said circuit design.

19. The method of claim 17, wherein said replacement table comprises:

a list of driver cells comprised of at least a portion of the gates in the design library used to create said circuit design;

a combination of each of said gates in said list of driver cells and a control to zero function;

a combination of each of said gates in said list of driver cells and a control to one function; and

a combination of each of said gates in said list of driver cells and an observe function.

20. The method of claim 19, wherein said replacement table further comprises gates in addition to gates in said design library including:

one or more combinations of a gates not in said design library and a control to zero function;

one or more combinations of a gates not in said design library and a control to one function; and

one or more combinations of a gates not in said design library and an observe function.

21. The method of claim 13, wherein the step of selecting a replacement cell from said accept list comprises selecting the potential replacement cell resulting in a circuit delay closest to the delay of the circuit with the driver cell.

22. The method of claim 13, wherein the step of selecting a replacement cell from said accept list comprises selecting the potential replacement cell having the smallest layout area.

23. The method of claim 13, wherein the step of selecting a replacement cell from said accept list comprises selecting the potential replacement cell having the smallest power requirement.

24. The method of claim 13, wherein the step of selecting a replacement cell from said accept list comprises selecting the potential replacement cell according to a user defined algorithm for combining the layout area and the power requirement of the potential replacement cell.